RESEARCHERID
THOMSON REUTERS

[Jain * *et al.*, 7(8): August, 2018]
IC™ Value: 3.00

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

DESIGN AND IMPLEMENTATION OF A MULTI STAGE SIGMADELTA ON CHIPADC WITH LOW OVERSAMPLING RATIO

Meenu Jain*[1] & Asst.Prof. Anupreksha Jain[2]

[*1]Student of MTECH (VLSI), ADINA Institute of Science and Technology, Sagar(M.P.)
[2]Asst.Prof. of VLSI department of (E&C), ADINA Institute of Science and Technology, Sagar(M.P.)

DOI: 10.5281/zenodo.1336717

ABSTRACT

A 16-bit pipelined analog-to digital device (ADC) is intended during this paper. The pipelined design realizes the high-speed and high-resolution. To cut back some complexities of flash ADC pipeline ADC is employed. The standardization schemes of pipelined ADC limit absolute and relative accuracy. Deviations in residue electronic equipment gain results because of low intrinsic gain of transistors, and mismatching between all the capacitors of capacitance 1pF lead to each deviations in residue electronic equipment gain and DAC nonlinearity in a much pipelined ADC. To image the planet, a low-power CMOS image sensing element array is needed within the vision processor. The image sensing element array is usually fashioned through pin diodes and analog to digital device (ADC). To attain low power acquisition, a low-power mid-resolution ADC is important. Digital correction permits conjointly to use terribly low power dynamic comparators. The multiplying D/A converters (MDACs) utilize a changed collapsed dynamic electronic equipment .In this allows to the employment of dynamic amplifiers in a very pipeline ADC. Additionally, the dynamic electronic equipment offers each clock measurability and high-speed operation even with a scaled offer voltage. exploitation the higher than techniques, a sixteen bit epitome ADC achieves a conversion rate of 407 MS/s with a offer voltage of 1.2 V. Therefore, the mixture of interpolated pipeline design and dynamic residue amplifiers demonstrates the practicability of ultra-low voltage high-speed analog circuit style. To implement the total system a low-power and tiny size capacitance worth sensing readout circuit is needed. Also, it's to be integrated along with the back-end low-power current-mode ADC on constant chip. The low-power current-mode ADC has been designed and unreal with TSMC 0.18um CMOS technology. Within the simulation result, the facility consumption for 16-bit ADC was ninety 1.9 microwatt, with an influence offer of 1.2 V.

Keywords: Galois field, cryptography, UART, cryptanalysis and linear error-correcting.

I. INRTODUCTION

Signal processing is very important in many of the system on-a-chip applications. With the advancement in technology, digital signal processing has gained significant importance in the field of telecommunication, biomedical, control systems and so on. This has necessitated the need for design of high precision data converters thereby attracting immense research in this field. Analog to digital converters (ADCs) is a mixed signal device that converts analog signals which are real world signals to digital signals for processing the information. In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Therefore the focus of this research is to design efficient low voltage ADCs that operate at high speed.

II. ADC PARAMETERS AND CHARACTERISTICS

1. Basic ADC concepts and terminology fundamentally analog to digital conversion involves sampling the analog signal and processing the sampled signal to generate the digital output bits. The rate at which the input signal is converted to its digital form determines the conversion speed and the number of output bits represents the resolution of the ADC. Some of the basic concepts of ADC are explained below. 1. Input Signal Bandwidth The frequency range of the input signal which can pass through the analog front end circuitry with minimal amplitude loss is called the bandwidth of input signal. For a sinusoidal signal, it is referred to as the frequency at which the amplitude is reduced by 70.7 % of original amplitude.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

2. Sample Rate The first step towards conversion of analog to digital is sampling. Sample rate or sampling frequency is defined as the number of samples of the input signal taken per second. According to the Nyquist theorem, for any band limited signal with maximum frequency Fmax, the sampling frequency must be at least equal to or greater than twice Fmax in order to reconstruct the signal properly. This implies that if the sampling frequency is less than twice Fmax, the signal cannot be reconstructed perfectly and higher the number of samples better would be its reconstruction.

3. Resolution The smallest amplitude change in the input signal that can be distinguished by an ADC is called resolution. This can be expressed in terms of full scale voltage of input, but is typically represented as the number of bits used to represent the output digital signal. Higher the number of output bits better is the resolution. For instance, a 4 bit ADC divides the input signal into sixteen levels while a 6 bit ADC divides the signal into sixty four steps consequently giving better resolution. The size of each step which is equal to LSB bit voltage is given by FSR/2N where FSR is the full scale range of the input.

4. Quantization Error While converting the analog signal to digital or in other words digitizing the analog signal, with a finite resolution ADC there exists a certain amount of uncertainty termed as quantization error or quantization noise. It is the difference between actual analog signal value and its quantized digital value.

5. Signal to Noise Ratio (SNR) By definition, SNR is the ratio of full scale value to the rms value of the quantization noise. The rms value is the root of mean of square of quantization noise. It is the measure of signal power relative to the noise power.

$$SNR = 10\ LOG\left(\frac{Psignal}{Pnoise}\right)$$

6. Effective Number of Bits (ENOB) ENOB is a measure of actual performance of an ADC, which gives the conversion bit of an ADC. ENOB is computed as shown below

$$ENOB = \frac{SNR\text{-}1.76}{6.02}$$

7. Spur-Free Dynamic Range (SFDR) SFDR is the ratio of the strength of the fundamental frequency to the strongest spurious signal in the output. It is an indicator of fidelity of an ADC. Nonlinearity in the ADC generates spurious signals that affect the achievable SFDR. SFDR can be calculated using the below formula

$$SFDR = Signal\ (dB) - \ largest\ spur(\ dB)$$

8. Differential non-linearity (DNL) DNL is a measure of separation between adjacent levels measured at vertical jump. DNL measures any deviation from one LSB.

9. Integral non-linearity (INL) INL is the maximum difference between actual finite resolution characteristic and ideal finite resolution characteristics.

III. ADC ARCHITECTURE

When coming up with ultra-low-power circuits, energy concerns drive the planning method from the choice of design to the particular circuit Implementation. Selecting design may be a crossroads within the style method for such systems. a correct selection of design will cause dramatic energy savings related with alternatives. Conversely, a poor result in a very sub-optimal style in spite of however well the individual circuit blocks are designed. Their energy feeding is greater during this application house,that area unit more than a few different concerns driving the selection of ADC design. Figure 5.1 teams numerous ADC architectures that change roughly by their accomplishable resolution, speed and power consumption [25]. Since low-power consumption is that the primary style Figure 5.1 shows that plentiful design area unit poor results. Time interleaved ADCs need multiple sets of analog hardware, resulting in high power consumption however in no time sampling rates [26]. Flash converters [27] use an outsized range of comparators.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

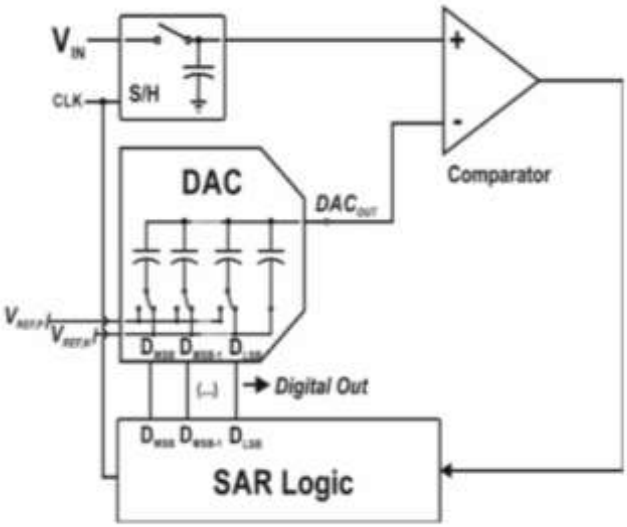
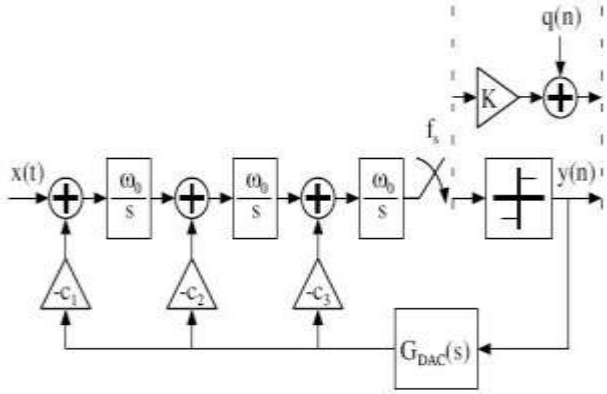


Figure 3.1 ADC Architectures.

To a given resolution, creation them impractical in greatest use requiring more than 8 bits of resolution. Folding and/or interruption [8] could help decrease the number of comparators required, but the architecture is not good suited for low-power requests. Multi-step 29] ADC also require a relatively bulky amount of analog hardware, resulting in excessive power consumption for application in distributed sensor networks less of the other ADC architectures, such as Delta-Sigma, Succeeding Estimate, Integrating and Algorithmic, has been reported to work with low-power consumption, low supply voltage and with modest resolution then speed [3]-[3]. Some of the already existing low–power architectures are reviewed.

1) Delta- Sigma ADC:



Number 3.2 Continuous-time 3rd order Σ Δ-modulator block figure [3].

Fig 3.2 shows the block figure of a third order low-pass Σ Δ ADC using a continuous time loop filter. The ADC [2] was reported to has a resolve of 10 bits and a dynamic range (DR) of 67 dB at a sampling rate of *f*s = 1.4MHz, though drawing an bias current of 60 μA to a modest supply voltage of 1.8V, thus consuming 108 μW of power. The ADC were intended to a 0.35-μm CMOS technology.

2) Successive Approximation:

Shown in Fig 4.3, the succeeding estimate architecture use only one comparator, along to simple digital logic and a switching network to instrument the search algorithm. The ADC [3] were designe to a 0.25 μm CMOS process and were report to consume 31pJ/8-bit sample at 1-V supply & 100 KS/s.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

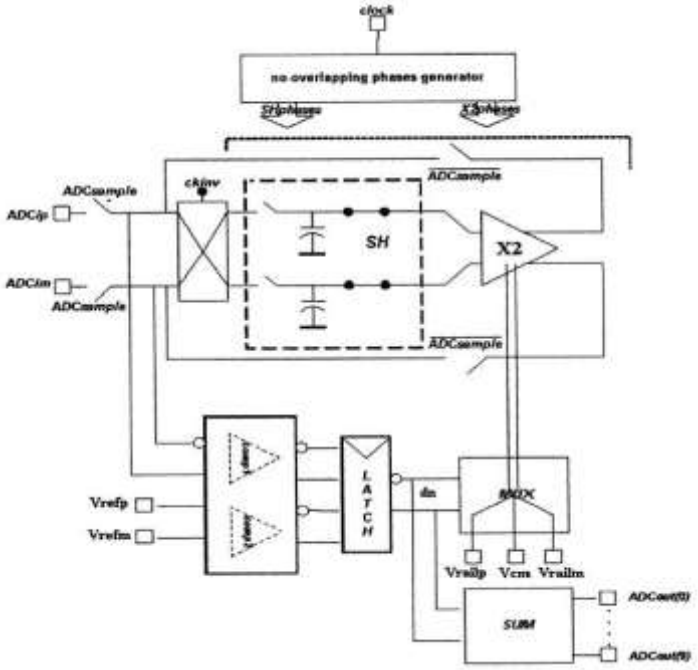


Figure 3.3 Successive approximation architecture [7]

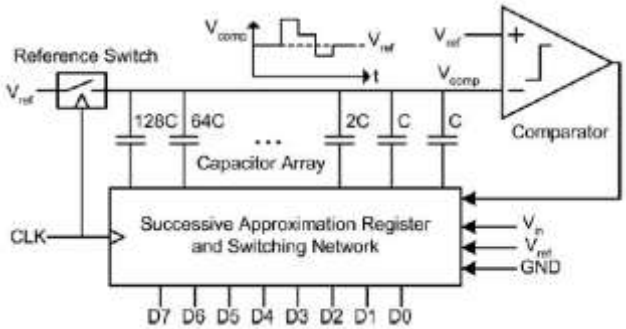


Figure 3.4 Algorithmic ADC schematic Diagram [4].

Over sampled converter adore sigma-delta converters square measure maybe viable to this application. Sigma-delta ADCs to often shape to be low-power [5] for a given resolve and rate, but they were complex–requiring refined time and filtering. The oversampled clock may be a lot of faster than the specified rate. Generating the oversampled clock in every detector node would doubtless offset any energy investments achieved within remainder of the ADC.

Continuing the survey of common architectures, integration (single and twin slope) converters [5] possess more of the specified study options. They necessity tiny analog electronic equipment, creating them awfully low-power. But they need right temporal arrangement which may be tough to attain while not a high precision clock. It is unlikely that such a clock would exist on the stuff since generating this clock might take quite a more of power because of the exactness need. Another disadvantage is that the conversion speed is extremely slow the variable conversion amount complicates the general system style for the detectornode as a whole as different ADC samples will take different amounts of time.

The charge distribution ordered approximation design [2], [3], [1] may be a viable design for this application house. the overall design of a general ordered approximation ADC sometimes consists of a rail-to rail analog comparator, a digital-analog converter and a ordered approximation register In general, the SAR is meant into

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

the digital electronic equipment. The DAC needed within the ADC is meant supported a R-2R ladder. Thus, each of them appropriate for the quality CMOS technology VLSI implementation. However, realizing high-accuracy and rail-to-rail MOS comparator at the same time remains a haul due to MOS device mismatches [5], [6] and threshold voltage limitations [7]. conjointly the accuracy of a ordered approximation convertor depends on the matching accuracy of the on-chip passive elements as a result of the convertor employs so as to take care of magnitude relation accuracy, such preciseness elements need an oversized space and can't be simply scaled down.

Algorithmic converters [6] offers all the benefit to the ordered approximation design, where merging full flexibility to decide on current because the info carrying amount. Current-mode circuits supply the benefits of inherent low-tension swing and no want for linear capacitors, as opposition that utilized in switched electrical condenser techniques for voltage-mode recursive ADC's.

Another advantage of recursive convertor block is that it are often simply continual to form a pipelined recursive convertor by merely inserting a current-mode sample and hold blocks (SH) in among every block [8] energy consumption depends on the quantity of block cascaded i.e. N, wherever N is that the range of bits of resolution desired within the ensuing conversion. Just, current-mode circuit techniques that method the active signals within the current domain are projected to style the current-mode ADC [9], [7], [1]. Thus, they're appropriate for low-tension applications. a 6-bit current-mode recursive ADC [9] with terribly little chip space and low-power indulgence, enhancements was required to additional scale back Thus, the current-mode recursive ADC was chosen and therefore the design was changed on work with low-tension and current offer on have low-power consumption. the planning conferred makes use of the transistors operative in sub threshold region, so the will work beneath low-tension and low current offer.

IV. SUBTHRESHOLD REGION

One of the novel options of the planning of the current-mode ADC projected during this project is that it consumes ultra-low-power. Such low-power consumption is often achieved by many techniques that makes low-tension application achievable. Few of those techniques are exploitation bulk-driven MOSFETs [8], floating gate MOSFETs [9] etc. however low-tension alone is not decent to realize ultra-low power, current consumption ought to even be down therefore the top of mentioned techniques generate other problem related to them, like higher input referred noise because of smaller trans electrical phenomenon. to realize ultra-low-power operation during this style, the transistors were operated in sub threshold or weak inversion region of operation So operation of MOSFET in this region, its modeling, its noise analysis and its leak problem need to be discussed.

4.1Operation in Sub threshold Region

Sub threshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below Vth (threshold voltage). The weak inversion region is seen in Fig.4.1 as the linear region of the curve (semilog plot) . In the weak inversion, the minority carrier concentration is small, but not zero.

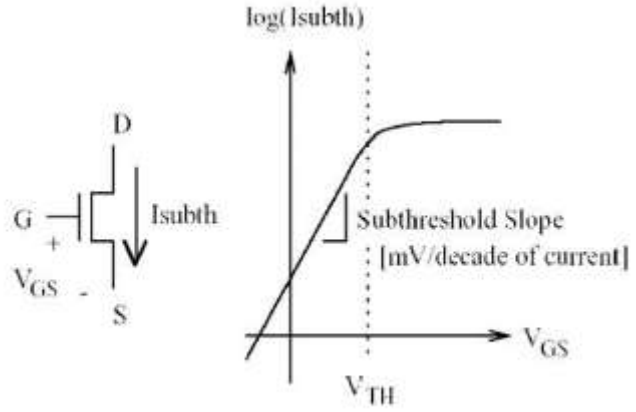


Figure 4.1 Sub threshold current in a NMOS transistor. The weak inversion region is shown as the linear region of the curve.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

4.2 Variation of minority carrier concentration in the channel of MOSFET biased in weak inversion.

The element of the electrical field vector E(Ey), being up to, $\partial\varphi/\partial y$ is additionally tiny. With each the quantity of mobile carriers and also the longitudinal force field tiny, the drift element of the sub threshold drain-to-source current is negligible. Therefore, the drift current dominates, the sub threshold physical phenomenon is dominated by the diffusion current. The carriers move by diffusion on the surface just like charge transport transversely the bottom of bipolar transistors. The exponential relation between driving voltage on the gate and also the drain current could be a line in a very semilog plot of ID versus Vg (see Fig. 5.1). Weak inversion generally dominates fashionable device off-state run because of the low Vth. The weak inversion current is expressed supported the subsequent [4]

$$I_{DS}=KP\frac{W}{L}(1+LAMBDA.V_{DS})(V_{GS}-V_{TH})^2$$

Where Vth is the threshold voltage, and υ_T =kT/q is the thermal voltage. Cox is the gate oxide capacitance; 0 is the zero bias mobility; and m is the sub threshold swing coefficient (also called body effect coefficient). Wdm is the maximum depletion layer width, and tox is the gate oxide thickness. Cdm is the capacitance of the depletion layer.

4.3 Modeling in Sub threshold Region

The accurate modeling of MOS transistors in moderate and weak inversion regions are not certain as moderate region is considered just a transition region through which one fits an approximate curve. So couple of tests should be performed to verify the modeling of the MOSFET, which was finding in accordance with the obligatory graphs. The graphs were obtained by simulating a NMOS transistor in Cascade, which drain were given a fixed dc bias, source was grounded and gate voltage was cleared over the entire range. The replication was performed so as to confirm if the MOS device is shown correctly for weak inversion region of operation. Fig 5.3 and Fig 4.4 confirmed the modeling. This were important since all the blocks in ADC are using transistors working in sub threshold region; hence the simulation performed on these blocks and as a result on the overall ADC will give the accurate results.

V. SIMULATION RESULTS

1. Design of basic comparater

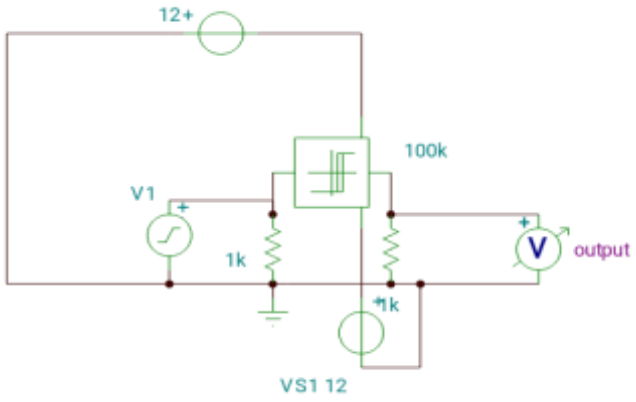


Fig (5.1) Basic comparator.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

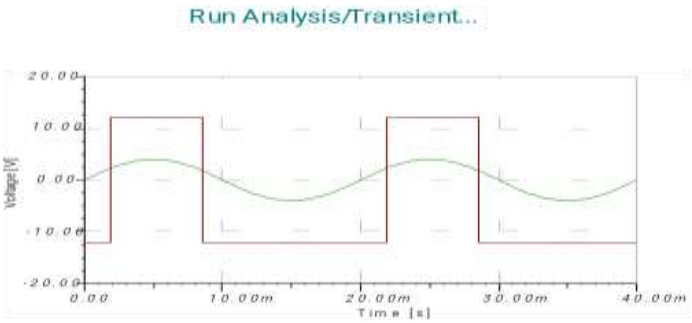


Fig (5.2) Voltage and time curve

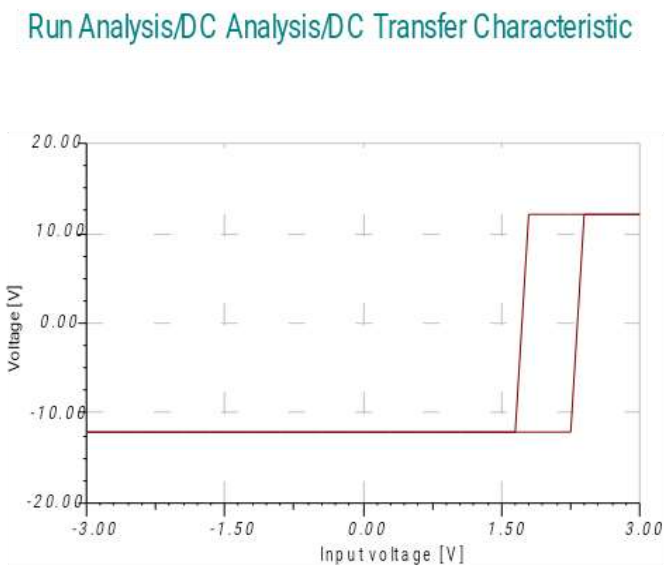


Fig (5.3) Run time analysis.

fig 5.2. Proposed circuit in adc:

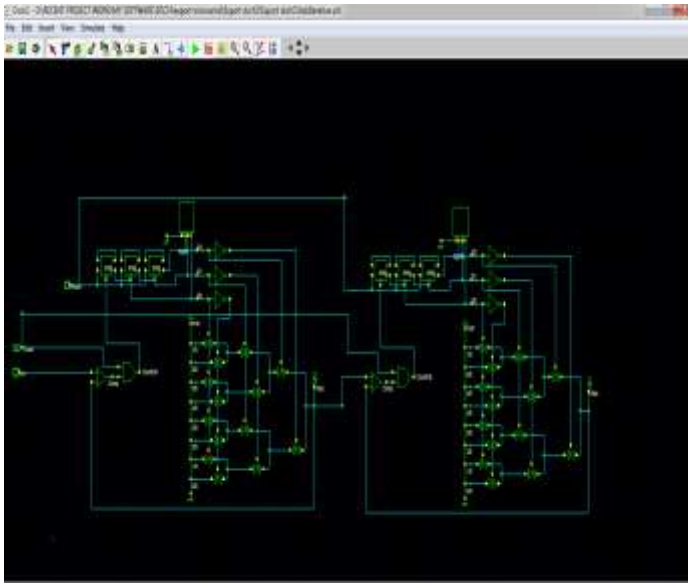


Fig 5.4 Pipelining in 16BIT Repeated Counter In ADC Display to Show 16bit Segment.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

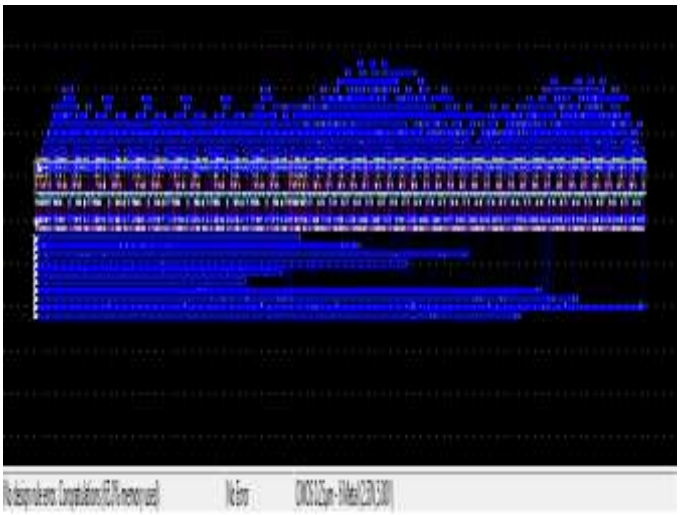


Fig (5.5) 16 Bit Pipeline in SAR ADC Layout.

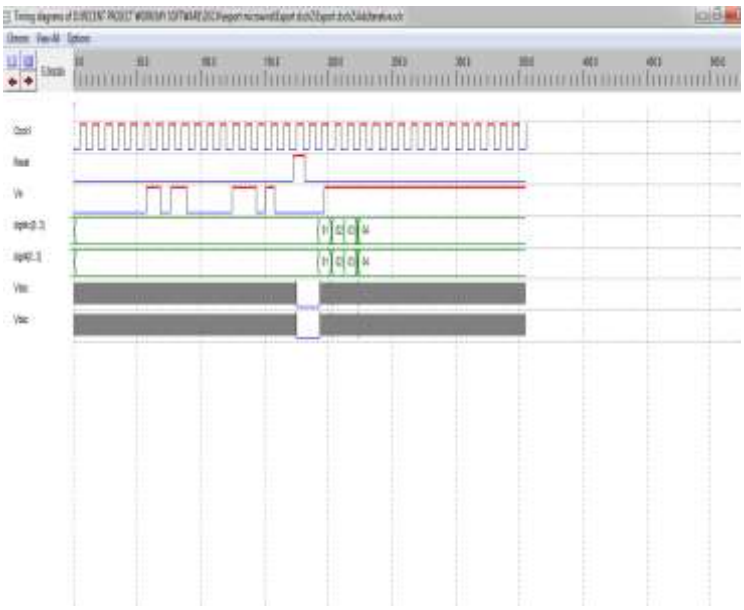


Fig.5.6 counter output in 16bit sar adc

1. The first graph presents the change in switching time with respect to variation in aspect ratio. It is important to see these results because it's the main thing which will affect the speed of the dynamic amplifier.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

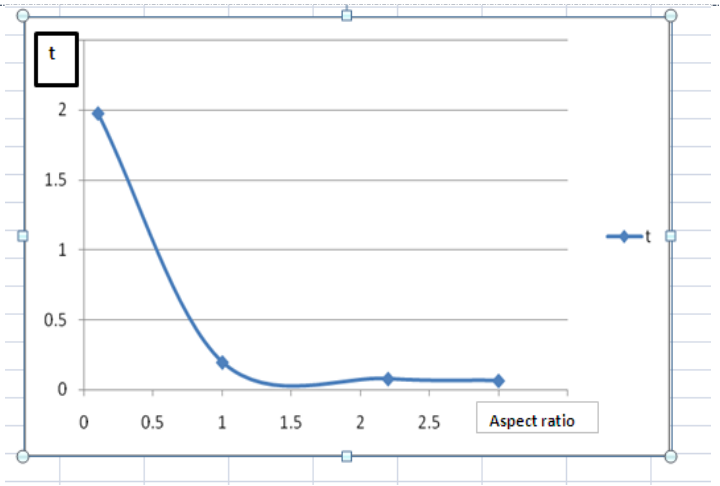


Fig 5.7 Graph between switching time & aspect ratio

From this graph it is very clear that as we increase value of aspect ratio the switching time decreases. Switching time is the time required to on or off the transistor. So that speed will increase because speed is indirectly proportional to time. For better results w=3l can be a good option.

2. This graph represents the relation between drain current and aspect ratio for three different materials Ge, Si and GaAs. Their motilities are different; other things are constant for them.

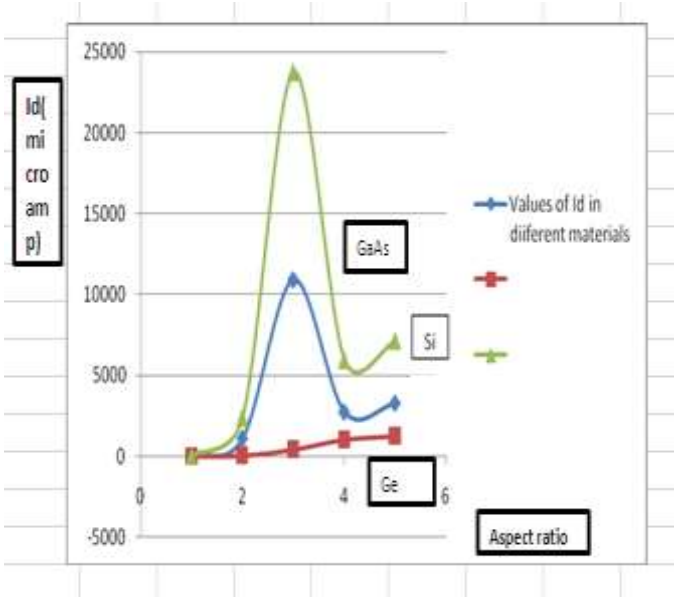


Fig 5.8 Graph represents Comparison of three elements based on mobility

From this graph we can observe that GaAs is the best because its curve reaches at max. Some results which are drawn from analysis are as follows;

- The threshold voltage for the dynamic amplifier is decreased.
- Power consumption naturally will reduce.
- The input impedance decreases to some content.
- Before the triggering was at5 V, now it is reduced to 3 V.
- RAM, ROM can be designed easily.

Applications

- ADC where we deal with very low voltage swings
- Micro strip antenna can be designed.
- High speed processor or controller can be designed.

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

VI. CONCLUSION

This enables the use of dynamic amplifiers in a pipeline ADC. In addition, the dynamic amplifier offers both clock scalability and high-speed operation even with a scaled supply voltage. Using the above techniques, a 16 bit prototype ADC achieves a conversion rate of 407 MS/s with a supply voltage of 1.2V. Therefore, the combination of interpolated pipeline architecture and dynamic residue amplifiers demonstrates the feasibility of ultra-low voltage high-speed analog circuit design. To implement the whole system a low-power and small size capacitance value sensing readout circuit is required. Also, it has to be integrated together with the back-end low-power current-mode ADC on the same chip. The low-power current-mode ADC has been designed and fabricated with TSMC 0.18um CMOS technology. In the simulation result, the power consumption for 16-bit ADC was 91.9 Microwatt, with a power supply of 1.2 V. The targeted specifications are met with the simulations in the schematic level and it has been shown that power consumption of the ADC using correlated level shifting is low.

REFERENCES

[1] International Technology Roadmap for Semiconductors, 2013 [Online]. Available: http://www.itrs.net.
[2] M.E.Sinangil,M.Yip,M.Qazi,R.Rithe,J.Kwong,andA.P.Chandrakasan,"Designoflow-voltage digital building blocks and ADCs for energy-efficient systems," IEEE Transaction on Circuits and Systems II:Express Briefs,vol.59,no.9,pp.533–537,Sept.2012.
[3] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," IEEE J. SolidState Circuits,vol.40,no.12,pp.2373–2387,Dec.2005.
[4] K.P.Pun,S.Chatterjee,and P.Kinget,"A0.5-V74-dBSNDR25-kHz continuous-time delta-sigma modulator with a return-to-open DAC," IEEEJ.Solid State Circuits, vol. 42, no.3, pp.496–507,Mar.2007.
[5] D. C. Daly and A. P. Chandrakasan, "A 6-bit, 0.2 V to 0.9 V highly digital flash ADC with comparator redundancy," IEEE J. Solid-State Circuits,vol. 44,no.11,pp.3030–3038,Nov.2009.
[6] P.J.A. Naus et. Al., "A CMOS Stereo 16-bit D/A converter for digital audio", IEEE J. of SolidState Circuits, vol.SC-22, No.3, pp.390-395,june 1987.
[7] F. W. Singor and W. M. Snelgorve, " Switched capacitor bandpass delta-sigma A/D modulation at 10.7MHz " , IEEE J. of Solid-StateCircuits, vol. 30, No.3, pp. 184-192, March 1995.
[8] B. Razavi, Design of Analog CMOS Integrated Circuits, New York McGraw-Hill, 2001.
[9] Galup-Montoro, C.; Schneider, M.C.; Loss, I.J.B.;, "Series-parallel association of FET's for high gain and high frequency applications," IEEE J. Solid-State Circuits, vol. 29, no. 9, September 1994.

Table 5.1 Table Compare to Various Research Papers

Architecture	Technology	Supply voltage	Sampling Rate	Power (mW)	Area (mm^2)
This work	**0.66-μm and 0.12 CMOS**	**1.2V**	**407MS/s**	**91.950Microwatt**	**0.792**
Interpolated pipeline architecture	**90 nm CMOS**	**0.55 V**	**160 MS/s**	**2.43**	**0.25**

ISSN: 2277-9655
Impact Factor: 5.164
CODEN: IJESS7

Successive Approximation Technique	**65nm & 90nm CMOS**	**1V & .5V**	**50MS/s**	**3.5 3.6**	**0.16**
Differential OPAMP Technique	**0.18-μm CMOS**	**1.8V**	**20MS/s**	**0.7**	**0.19**
Folded Cascade Technique	**0.18-μm CMOS**	**1.8V**	**230 MS/s**	**270**	**1.97**
switched-opamp technique	**0.5-μm CMOS**	**1.5**	**5MS/s**	**1.6**	**1.3**

CITE AN ARTICLE

Jain, M., & Jain, A., Asst. Prof. (2018). DESIGN AND IMPLEMENTATION OF A MULTI STAGE SIGMADELTA ON CHIPADC WITH LOW OVERSAMPLING RATIO. *INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY*, *7*(8), 177-187.